

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

James Chambers

Serial No.: N/A

Filed: Herewith

For: STRUCTURE AND METHOD TO FABRICATE SELF-ALIGNED
TRANSISTORS WITH DUAL WORK FUNCTION METAL GATE
ELECTRODES

Group No.: N/A

Examiner: N/A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

U.S. Patent No.
6,534,423 B1
6,397,861 B1
6,383,879 B1

Inventor
Turner
Wing et al.
Kizilyalli et al.

Date
March 18, 2003
June 4, 2002
May 7, 2002

Foreign Patent No.
GB 2 347 789 A

Country
UK

Date
September 13, 2000

References:

"PURSUING THE PERFECT LOW-K DIELECTRIC";
www.e-insite.net/semiconductor/index.asp?/layout=articlePrint&articleID=CA164243.

B. Maiti and P.J. Tobin; "METAL GATES FOR ADVANCED CMOS TECHNOLOGY";
SPIE Vol. 3881; September 1999; Pgs. 46-57.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 20-0668.

Respectfully submitted,

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Date: 8/27/03

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Completion if Known	
				Applicant Number	N/A
				Filing Date	Herewith
				First Named Inventor	James Chambers
				Art Unit	N/A
				Examiner Name	N/A
Sheet	2	of	2	Attorney Docket Number	TI 35714

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"PURSUING THE PERFECT LOW-K DIELECTRIC"; www.e-insite.net/semiconductor/index.asp?layout=articlePrint&article ID=CA164243	
		B. Maiti and P.J. Tobin; "METAL GATES FOR ADVANCED CMOS TECHNOLOGY"; SPIE Vol. 3881; September 1999; Pgs. 46-57.	

Examiner Signature		Date Considered	
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	N/A
Filing Date	Herewith
First Named Inventor	James Chambers
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	TI 35714

Sheet	1	of	2
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U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				
		GB 2 347 789 A	09/13/2000	NEC Corporation		

Examiner Signature		Date Considered	
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